

Nanochannel diodes based on InAs/Al₈₀Ga₂₀Sb heterostructures: Fabrication and zero-bias detector properties

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The authors present a novel process for fabrication of deep submicron isolation patterns in InAs/Al₈₀Ga₂₀Sb heterostructures. The process is demonstrated by processing InAs/Al₈₀Ga₂₀Sb self-switching diodes (SSDs). SSDs require high-resolution isolation patterns, which presents a major fabrication challenge because of the oxidation sensitivity of Al(Ga)Sb alloys. The presented fabrication process completely avoided exposure of Al(Ga)Sb to air and resulted in an isolation pattern with a feature size down to 35 nm. The process was based on a dry etch of isolating trenches, *in situ* removal of the resist etch mask followed by *in situ* encapsulation of etched surfaces by silicon nitride. The applicability of the InAs/Al₈₀Ga₂₀Sb SSD process was demonstrated with on-wafer RF measurements of zero-bias detection up to 315 GHz. Below 50 GHz, the detector's noise-equivalent power was estimated to less than 100 pW/Hz^{1/2}. © 2015 American Vacuum Society.

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I. INTRODUCTION

In the family of III–V materials, InAs is characterized by its high electron saturation velocity (4×10^7 cm/s) and low band gap (0.42 eV).¹ InAs has a large conduction band offset to AlSb (1.35 eV). Hence, the InAs/AlSb heterojunction is utilized in a series of microwave and optical devices such as resonant-tunneling diodes,² interband backward diode detectors,³ infrared quantum cascade lasers,⁴ and high-electron-mobility transistors (HEMT).⁵

Another type of device demonstrated in similar heterostructures is the self-switching diode (SSD) detector.⁶ We have reported on an InAs/Al₈₀Ga₂₀Sb SSD detector with a voltage responsivity of 34 V/W and noise-equivalent power (NEP) of 65 pW/Hz^{1/2} when operated as a zero-bias direct detector at 50 GHz.^{6,7} Detection was also demonstrated at 600 GHz.⁶ Fabricating the InAs/Al₈₀Ga₂₀Sb SSDs in Refs. 6–8 required special processing techniques, which are the focus of this paper.

SSDs require a lateral design of nanometer-sized channels and highly isolating trenches.^{7,9,10} Al(Ga)Sb is well known to be chemically unstable and very prone to oxidation,¹¹ which makes the fabrication of isolation patterns with deep submicron features extremely challenging. Ion implantation has been shown to provide excellent mesa isolation for InAs/AlSb HEMTs without exposure of Al(Ga)Sb layers.⁵ However, ion implantation isolation relies on disruption of the crystal lattice, which results in semi-isolated regions with a lateral width of several hundreds of nanometers.¹²

While a nonabrupt transition to isolating regions causes no issues for mesa isolation, it effectively prevents the definition of nanometer-sized isolation patterns necessary for SSD fabrication.

In this paper, we present a processing technique for deep-submicron isolation patterns in InAs/Al₈₀Ga₂₀Sb SSDs. The fabrication employs an etching technique to achieve isolation with high resolution while keeping Al(Ga)Sb layers protected from air. The technique is a development of a previously published method for *in situ* (i.e., without breaking the vacuum) encapsulation and passivation of etched InAs/Al₈₀Ga₂₀Sb structures where silicon nitride was subject to a lift-off process.¹³ In the present study, the resist mask is removed *in situ*, which strongly enhances the line resolution as compared to previous methods.¹² Isolating trenches are achieved through a combination of dry-etching, *in situ* resist removal, and *in situ* encapsulation of trenches using a virtually arbitrarily thick silicon nitride layer, thus completely avoiding sample exposure to air. Sensitive AlSb layers in the heterostructure are replaced with the chemically more stable alloy Al₈₀Ga₂₀Sb.¹⁴ As a result, we are able to fabricate 35 nm isolation patterns in InAs/Al₈₀Ga₂₀Sb SSDs. The SSDs are demonstrated in zero-bias detector experiments up to 315 GHz.

II. EPITAXIAL STRUCTURE AND DEVICE DESIGN

The SSDs were fabricated on a 15×15 mm² sample grown by molecular beam epitaxy on a two inch GaAs substrate. The epitaxial layers are shown in Table I. Growth began with a 300 nm GaAs smoothing layer after thermal deoxidation of the GaAs substrate. A 1 μm metamorphic

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TABLE I. Epitaxial structure of the fabricated InAs/Al₈₀Ga₂₀Sb SSDs.

Layer	Material	Thickness (nm)
Cap layer	InAs:Te	5
Protection layer	In ₅₀ Al ₅₀ As	4
Barrier	Al ₈₀ Ga ₂₀ Sb	13
Channel	InAs	15
Buffer	Al ₈₀ Ga ₂₀ Sb	100
Metamorphic buffer	AlSb	1000
Smoothing layer	GaAs	300
Substrate	S.I. GaAs (001)	

AlSb buffer was grown to relax the strain due to the difference in lattice constant (5.65 and 6.06 Å for GaAs and InAs, respectively).¹⁵ Al₈₀Ga₂₀Sb is more stable than AlSb, but also more conductive.¹⁶ As a trade-off between stability and isolation, 100 nm Al₈₀Ga₂₀Sb was selected for the top part of the buffer, forming the quantum well with the 15 nm InAs channel and 13 nm Al₈₀Ga₂₀Sb barrier. Finally, a 4 nm In₅₀Al₅₀As protection layer and an InAs cap layer with $6 \times 10^{18} \text{ cm}^{-3}$ Te-doping was grown.

In the active areas of the SSDs, the cap layer was etched away and the surface passivated with silicon nitride. Carrier concentration and electron mobility of such etched and passivated areas was in Hall measurements measured to $1.5 \times 10^{12} \text{ cm}^{-2}$ and $26\,000 \text{ cm}^2/\text{Vs}$, corresponding to a sheet resistance of $165 \, \Omega/\text{sq}$. Comparable values have been observed by others in similar structures.¹⁵

The design of the fabricated SSDs is illustrated in Fig. 1. Dark fields in Fig. 1 represent trenches etched down to the buffer layer, thereby creating an isolating structure. Current flows through nanometer-sized channels of width W modulated by neighboring flanges connected to the drain, acting as gates.¹⁷ These flanges are isolated from the active channels by trenches of width W_h and W_v . In a detector application, SSDs benefit from keeping both W and W_v as small as possible which creates a demand for a high-resolution isolation pattern.⁷ In this experiment, every SSD design had $N=43$ channels in parallel, with channel lengths $L=1000 \text{ nm}$, and the trench widths $W_h=W_v=100 \text{ nm}$. Devices with $W=50 \text{ nm}$ and $W=35 \text{ nm}$ were fabricated.

III. DEVICE FABRICATION

Fabrication started with the formation of Pd/Pt/Au ohmic contacts, defined in a lift-off process, deposited through

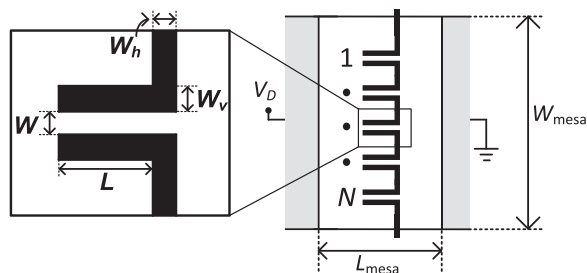


FIG. 1. Schematic top-view of the InAs/AlSb SSD design. Dark fields indicate isolating trenches.

electron-beam evaporation and annealed for 15 min at $275 \, ^\circ\text{C}$ in an H_2/Ar (1:9) atmosphere. Contact resistance was measured to $0.22 \, \Omega/\text{mm}$ using the transfer length method. After the ohmic contacts, Ti/Au metal pads were fabricated using lift-off and electron beam evaporation.

The fabrication of the trenches and mesas is illustrated in Figs. 2(a)–2(d). As illustrated in Fig. 2(a), the process started by etching a recess in the cap layer in the active area of the device using a $\text{C}_6\text{H}_8\text{O}_7/\text{H}_2\text{O}_2$ (1:1) solution. By stopping the etch in the In₅₀Al₅₀As protection layer, the Al₈₀Ga₂₀Sb layer remained encapsulated.

For the critical formation of the isolating trenches, an Oxford Plasmalab System 100 was used; a dual-chamber system with capability of both reactive ion etch (RIE) and inductively coupled plasma (ICP). The trenches were patterned in resist (ZEP520A) through e-beam lithography, see Fig. 2(b). Trenches were etched in the first chamber with a

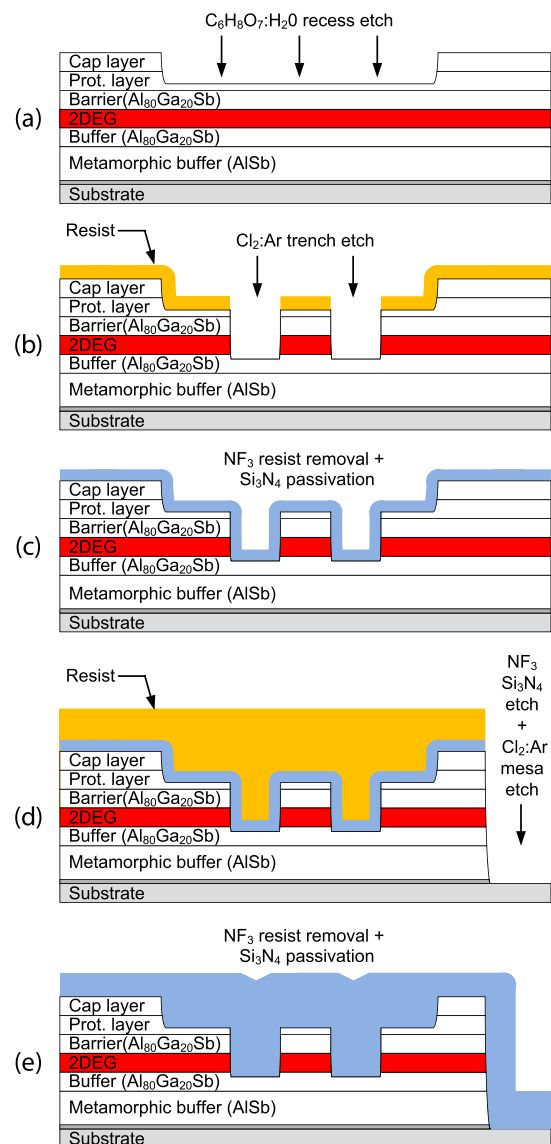


FIG. 2. (Color online) Schematic illustration of the InAs/AlSb SSD trench and mesa formation. (a) Recess etch, (b) trench etch, (c) *in situ* resist removal and temporary silicon nitride passivation, (d) silicon nitride removal and mesa etch, and (e) resist removal and final silicon nitride passivation.

highly directional Cl₂:Ar RIE process (15:15 sccm, 2 mTorr, 170 W electrode power, 460 V DC self-bias) to just below the InAs channel, stopping in the Al₈₀Ga₂₀Sb buffer, see Fig. 2(b). The resist was then removed *in situ* (i.e., without breaking the vacuum) using an NF₃ RIE process in the second chamber (20 sccm, 30 mTorr, 30 W electrode power, 20 V DC self-bias), which does not etch III–V semiconductors.¹⁸ In the next step, shown in Fig. 2(c), a layer of 25 nm silicon nitride was grown *in situ* in the second chamber by SiH₄:N₂:Ar plasma enhanced chemical vapor deposition (4:10:25 sccm, 2 mTorr, 100 W coil power, and no DC self-bias) to temporarily encapsulate and electrically passivate the etched surfaces. Thus, the oxidation-prone Al₈₀Ga₂₀Sb and AlSb layers were never exposed to air in the whole trench formation process.

After the trench fabrication, mesas for device isolation were patterned and the resist developed. Active device areas and metal pads remained covered by resist. The 25 nm silicon nitride layer was etched using the aforementioned NF₃ RIE process, see Fig. 2(d). Then followed a process similar to that of the isolating trenches: the sample was etched down to the GaAs substrate with a Cl₂:Ar RIE/ICP process (15:15 sccm, 2 mTorr, 100 W electrode power, 150 W coil power, and 300 V DC self-bias) to prevent excessive leakage through the Al₈₀Ga₂₀Sb buffer. The 90 s etch was performed in steps of 30 s with 30 s pauses to avoid thermal hardening of the resist. As shown in Fig. 2(e), the remaining resist was etched away with the NF₃ RIE process, also removing the 25 nm silicon nitride previously deposited to protect the etched trenches. A new, 180 nm thick silicon nitride layer was then grown with the previously mentioned process, completely filling the etched trenches and covering the mesa sidewalls. As the last step of the fabrication, probe openings in the passivation were etched through the NF₃ RIE process.

IV. PHYSICAL CHARACTERIZATION

The top-view scanning electron micrograph (SEM) image of an SSD in Fig. 3 was taken after the isolating trenches were etched and temporarily passivated, i.e., corresponding to the process step in Fig. 2(c). Clearly defined and

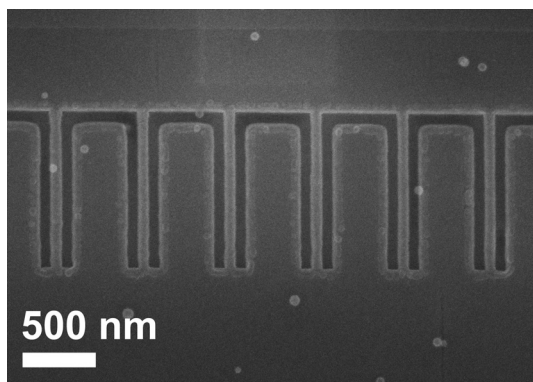


Fig. 3. SEM of isolating trenches after temporary encapsulation and passivation with a 25 nm silicon nitride layer. The imaged InAs/AlSb SSD channels were designed for channel width $W = 45$ nm.

uniformly etched trenches are observed in Fig. 3, indicating that the process allows narrower trenches than 100 nm.

A scanning transmission electron microscopy (STEM) cross section of an etched channel is shown in Fig. 4. The trench etch reached through the InAs layer, isolating channels from the rest of the mesa. Isolation resistance of the etched trenches was measured across a 100 nm wide trench to more than 1 GΩ/sq. In Fig. 4, the designed channel width W was 50 nm, which corresponds well with the width of the top of the InAs layer observed in the STEM picture. However, Fig. 4 shows that the cross section of the InAs channel was trapezoidal with a 70 nm wide base. On top of the channel is the Al₈₀Ga₂₀Sb barrier, slightly overetched in the trench etch process. The width of the Al₈₀Ga₂₀Sb barrier was 35 nm, 15 nm narrower than the top of the InAs channel and the designed W . Furthermore, Fig. 4 shows that vertical dimensions are as specified in the heterostructure design listed in Table I. The designed thickness of the Al₈₀Ga₂₀Sb barrier was 13 nm. The dark layer on top of the InAs channel in Fig. 4 was slightly higher than 13 nm, implying that only a thin (1–2 nm) of the In₅₀Al₅₀As protection layer remained.

InAs/Al(Ga)Sb heterostructures are expected to exhibit elongated defects in the [1–10] direction.¹⁹ Such defects can be seen in the inset of Fig. 4, running perpendicularly to the plane of the cut. To maximize InAs channel electron mobility, the fabricated SSD channels were designed to run in parallel to the defects.²⁰

V. ELECTRICAL CHARACTERIZATION

DC-measurements of the same InAs/Al₈₀Ga₂₀Sb SSD as depicted in the STEM image in Fig. 4 are provided in Fig. 5. An equivalent circuit for the SSD⁷ is shown as an inset in Fig. 5. Here, R_i denotes the small-signal resistance of the active part of the channels of length L as noted in Fig. 1. The parasitic part of the channel is found as $R_{s2} = R_i W_v / L$. R_{s1} was measured to 40 Ω.⁷ Furthermore, $\gamma_i = (d^2 I_D / dV_{D_i}^2) / (dI_D / dV_{D_i})$ is the intrinsic DC curvature, where $V_{D_i} = V_D - I_D(R_{s1} + R_{s2})$. At low frequencies, the capacitance C_h can be ignored when extracting R_i . The voltage responsivity of

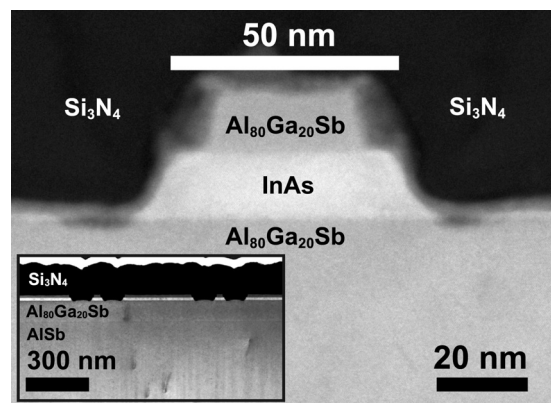


Fig. 4. STEM cross section of an InAs/AlSb SSD channel with designed channel width $W = 50$ nm cut along the [110] direction. The trenches reached just through the InAs channel. The inset shows dislocations running in the [1–10] direction, perpendicular to the plane of the cut and parallel to the fabricated channels.

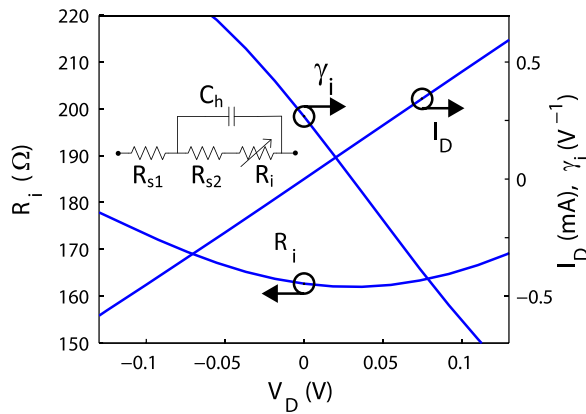


FIG. 5. (Color online) DC-measurements of I_D , γ_i , and R_i in a $W = 50$ nm InAs/AlSb SSD. Inset shows an equivalent circuit of an SSD (Ref. 7).

an SSD with a conjugately matched source is then found as $\beta_{\text{opt}} = R_i^2 \gamma_i / (2R_0)$, where R_0 is the total zero-bias resistance.²¹ Figure 5 illustrates that for $V_D = 0$ V, γ_i is nonzero. This enables zero-bias detection in the InAs/Al₈₀Ga₂₀Sb SSDs. More qualitatively, the asymmetric R_i , lower for forward bias than for reverse bias, illustrates the rectifying behavior of the InAs/Al₈₀Ga₂₀Sb SSDs.

Zero-bias resistance R_0 and zero-bias conductance $1/R_0$ are plotted versus W in Fig. 6. R_0 can approximately be described as a function of the form $R'_0 = a + b/(W - W_o)$, where a , b , and W_o are constants found by fitting R'_0 to R_0 by the least-squares method. It may be noted that while R_i and R_{s2} are inversely proportional to $(W - W_o)$, also R_{s1} may vary with $(W - W_o)$ due to current crowding at the channel entrances. Extrapolating R'_0 in Fig. 6 shows that $1/R_0$ is expected to reach zero at $W = W_o = 16$ nm. The InAs surface exhibits either accumulation or depletion.²² A positive W_o indicates that in the case of the fabricated InAs/Al₈₀Ga₂₀Sb SSDs (passivated by silicon nitride), a depletion layer is formed at the channel sidewalls which act to make the effective channel width slightly smaller than the physical channel width. Since responsivity in SSDs is enhanced for narrow effective channels, an effective channel width

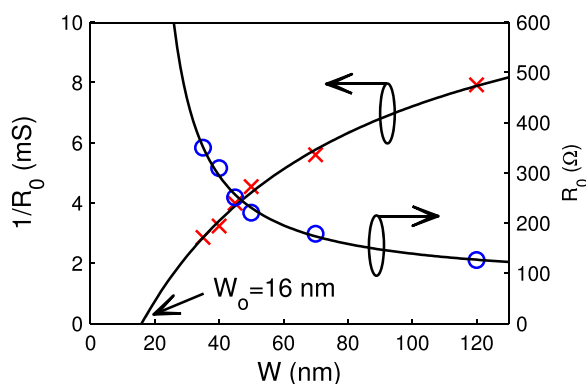


FIG. 6. (Color online) Zero-bias resistance R_0 (circles) and zero-bias conductance $1/R_0$ (crosses) as a function of W for the fabricated InAs/AlSb SSDs. Modeled R_0 and $1/R_0$ (solid lines) were used to determine the depletion width W_o .

smaller than the physical width is beneficial to the SSD in detector applications.⁷

Zero-bias voltage responsivity β_{opt} for InAs/Al₈₀Ga₂₀Sb SSDs with two different W is shown in Fig. 7(a). The device with $W = 50$ nm is the same device as depicted in the STEM-pictures in Fig. 4. To find β_{opt} , the zero-bias voltage responsivity with a 50Ω source ($\beta_{50\Omega}$) was measured on-wafer using a vector network analyzer as a signal source. $\beta_{50\Omega}$ was measured in three different bands (2–50, 140–200, and 220–315 GHz) using three different setups. β_{opt} was then calculated as $\beta_{\text{opt}} = \beta_{50\Omega} / (1 - |S_{11}|)$, where S_{11} of the SSDs was obtained from S-parameter measurements. Details of the measurement and $\beta_{50\Omega}$ of the $W = 35$ nm device are given in Ref. 6.

As demonstrated in Fig. 7(a), β_{opt} of the InAs/Al₈₀Ga₂₀Sb SSDs is higher for $W = 35$ nm than for $W = 50$ nm. It has been shown previously that β_{opt} is higher in InAs/Al₈₀Ga₂₀Sb SSDs with small W .⁷ Further, Fig. 7(a) illustrates a stronger roll-off of β_{opt} in the $W = 35$ nm device than in the $W = 50$ nm device: The $W = 50$ nm device exhibits a 60% lower β_{opt} at 2 GHz and 30% lower β_{opt} at 315 GHz. The stronger roll-off in β_{opt} for shorter W is explained by similar parasitic capacitances in the two devices whereas R_i is higher for small W .⁸

For low incident powers and zero bias current, Johnson noise is the dominating noise process.²³ Hence, the NEP for a conjugately matched SSD can be calculated as $\text{NEP}_{\text{opt}} = \sqrt{4kTR_0} / \beta_{\text{opt}}$, where k is Boltzmann's constant and $T = 290$ K the physical temperature. R_0 for the $W = 35$ nm and $W = 50$ nm devices in this experiment were 348 and 220Ω , respectively.

Figure 7(b) shows NEP_{opt} of the two devices with $W = 35$ and 50 nm. As a consequence of the β_{opt} roll-off at high frequencies, NEP_{opt} increases with frequency for both devices. While NEP_{opt} at 2 GHz is around 50% lower for $W = 35$ nm than for $W = 50$ nm, the difference at 315 GHz is only 15%. The convergence of NEP_{opt} for the two devices at high frequencies is a consequence of R_0 being lower for $W = 50$ nm than for $W = 35$ nm, whereas the latter exhibits a stronger roll-off in β_{opt} .

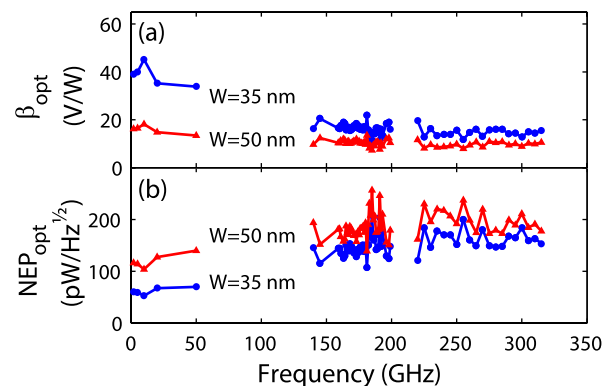


FIG. 7. (Color online) (a) Voltage responsivity β_{opt} of InAs/Al₈₀Ga₂₀Sb SSDs with $W = 35$ nm (dots) and $W = 50$ nm (triangles) when driven by a conjugately matched source and (b) estimated noise-equivalent power NEP_{opt} .

VI. DISCUSSION

The heterostructures used for fabricating the InAs/Al₈₀Ga₂₀Sb SSDs contains a two-dimensional electron gas and bears strong resemblance to what is used for InAs/AlSb HEMTs.⁵ Heterostructures similar to those used for HEMTs have also been utilized in SSDs made from InGaAs/InAlAs,²³ GaAs/AlGaAs,²⁴ GaN/AlGaN (Ref. 6) heterostructures. Producing SSDs in HEMT-like structures allows various methods for HEMT fabrication to be transferred to SSDs. The critical step in SSD fabrication in general, and for InAs/Al₈₀Ga₂₀Sb heterostructures, in particular, is the formation of isolating trenches with as high resolution as possible, which is the focus of this paper.

Different techniques for isolation in SSDs have been employed in other material systems. In InGaAs/InAlAs SSDs and GaAs/AlGaAs SSDs, the isolating trench is formed by a wet etch reaching the isolating buffer.^{23,24} The same technique is used for isolation in InP and GaAs HEMTs.^{25,26} In GaN/AlGaN HEMTs,²⁷ as well as GaN/AlGaN SSDs,⁹ ion implantation have been used to create isolation. As mentioned in Sec. I, ion implantation is especially attractive for oxidation-prone InAs/AlSb heterostructures but unfortunately provides limited resolution making it difficult to apply for InAs/Al₈₀Ga₂₀Sb SSDs.

The fabrication technique presented in this paper is a development of another approach to isolation in InAs/AlSb structures presented in Ref. 13. In Ref. 13, InAs/AlSb HEMTs were fabricated through a dry etch down to the Al₈₀Ga₂₀Sb buffer followed by an *in situ* encapsulation with 25 nm silicon nitride, and superfluous silicon nitride was removed in a lift-off process. Thicker silicon nitride layer means less oxidation, which is even more important for nanometer structures. In order to perform the lift-off process in Ref. 13, the thickness of the silicon nitride was limited to 25 nm and large (>1 μm) patterns. In contrast, the *in situ* resist removal and deposition described in this work allowed channel widths down to 35 nm to be defined and virtually any thickness of silicon nitride to be deposited.

VII. CONCLUSION

A technique for producing deep submicron isolation patterns in InAs/Al₈₀Ga₂₀Sb heterostructures was presented. To demonstrate the process, InAs/Al₈₀Ga₂₀Sb self-switching diodes were fabricated. Isolation was achieved through combining dry-etch of shallow and narrow trenches, *in situ* removal of the resist mask followed by an *in situ* growth of silicon nitride. The presented fabrication process avoided exposure of oxidation-prone Al(Ga)Sb alloys to air. The *in situ* removal of the resist etch mask allowed silicon nitride of virtually any thickness to be deposited, and nanometer-sized features to be etched. Fabricated InAs/Al₈₀Ga₂₀Sb SSDs

featured 100 nm wide isolating trenches separated by 35 nm broad channels. The SSDs exhibited a noise-equivalent power of less than 100 pW/Hz^{1/2} below 50 GHz.

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